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3	Realistion of Half adder and full adder		10/10/23	10/10/23	
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Aim: To study and verify the truth table of logic gate

objective: Identify various circuit and their specifications

(a) And gate (d) NAND gate
(b) OR gate (e) XNOR gate
(c) NOR gate (f) XOR gate

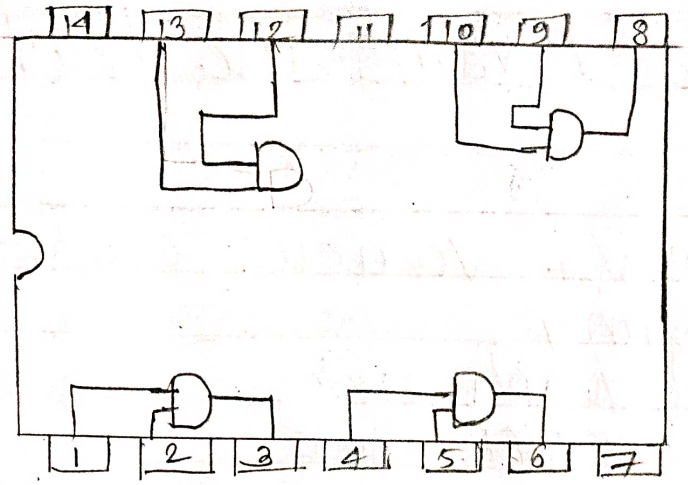
Apparatus: Breadboard connection wires IC 7400 IC 7432, IC 7406, IC 4702, IC 7404, IC 7486

Theory:

The basic logic gates are building blocks of more computer logic circuit. These logic gates perform the basic Boolean function such as And, OR, NAND, NOR, Inversion XOR, XOR, fig 1.1 shows the circuit symbol Boolean function such as And, OR, NA and truth. It is seen that each gate has one or two binary input A and B and one binary output C. The small circle on the output of the circuit symbols designates the logic complement. The AND, OR, NAND and NOR gates can be extended to have more than two inputs

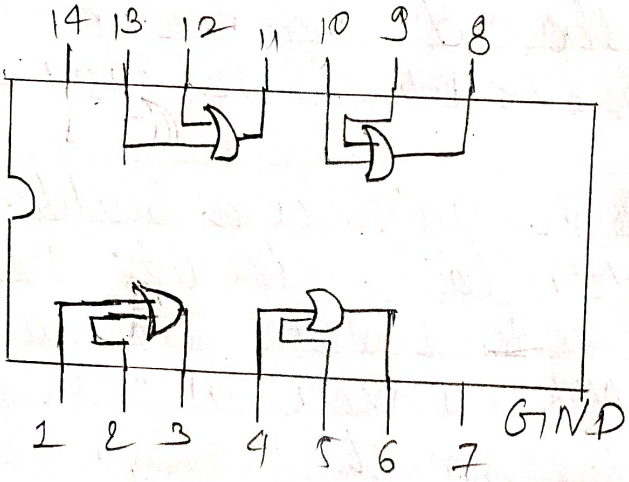
Teacher's Signature : _____

AND Gate



IC 7408

OR Gate



Ic7432

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AND gate: It is a digital circuit that has two or more inputs and produces an output which is the logical AND of all those inputs.

OR gate: It is a digital circuit that has two or more inputs and produce an output which is the logic OR of all those input. This logical OR is represented with the symbol '+'.

Not gate: It is a digital circuit that has single input and single output. This output of NOT gate is the logical inversion of input. Hence NOT gate is also called as inverter.

NAND gate: It is a digital circuit that has two or more inputs and produces an output which is inversion of logical AND of all those inputs

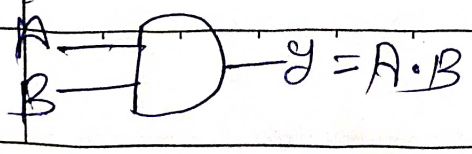
Truth Table

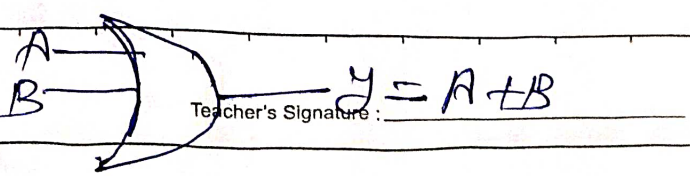
AND gate

A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

OR gate

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1





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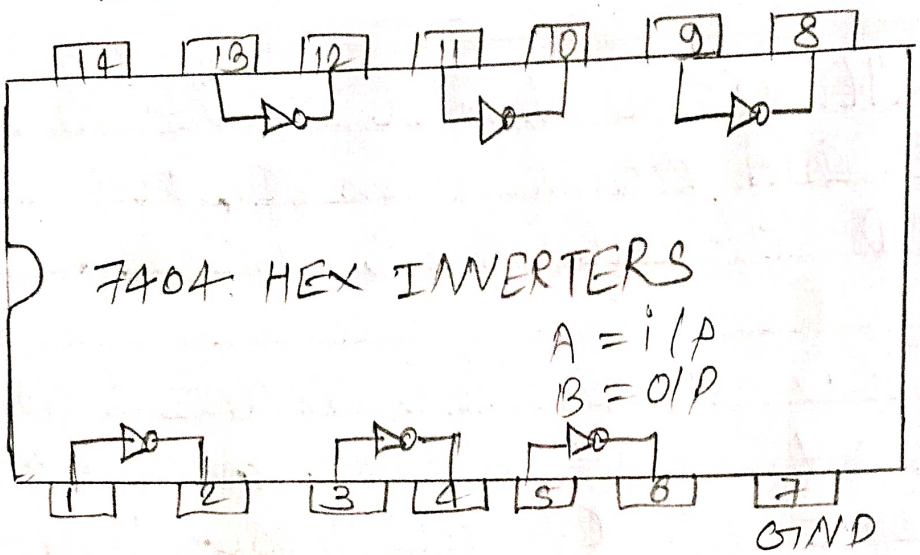
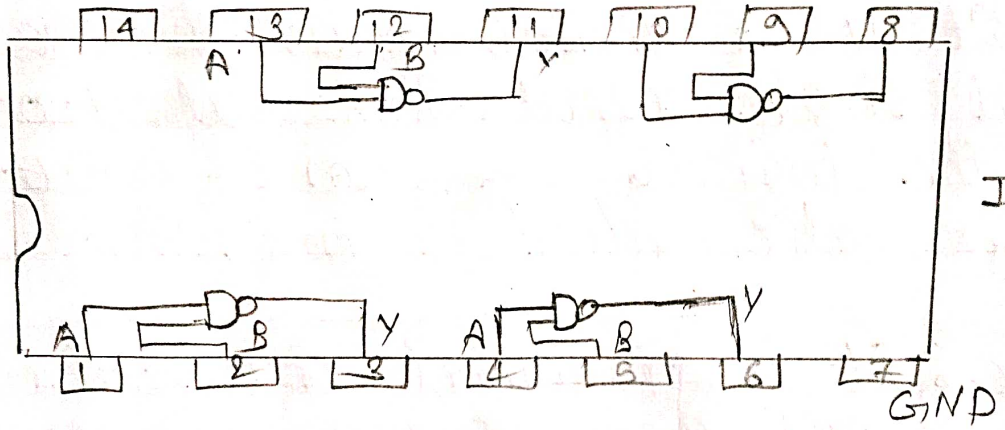
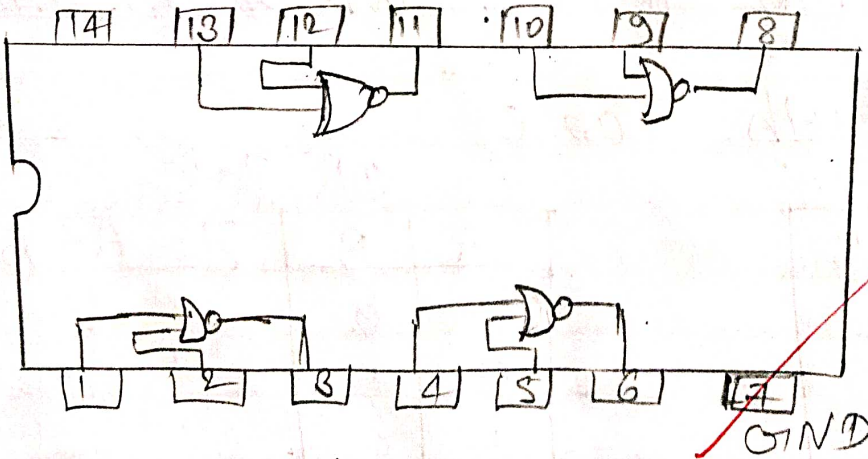
NOT Gate



NAND GATE





NOR gate

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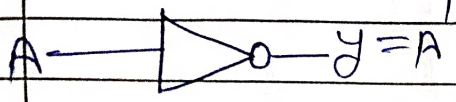
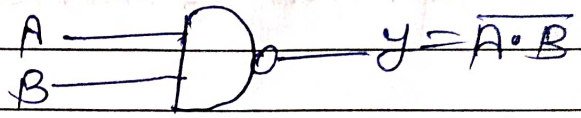
NOT gate

A	$y = A'$
0	1
1	0



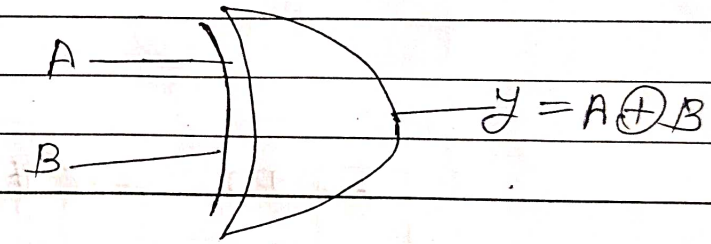
NAND gate

A	B	$y = A \cdot B' + A' \cdot B$
0	0	1
0	1	1
1	0	1
1	1	0



NOR gate: It is a digital circuit that has two or more inputs and produce an output, which is inversion of logical OR of all those inputs.

A	B	$y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



EX-OR gate: The full form of EX-OR gate is Exclusive-OR gate. Its function is same as that of OR gate except for some cases. When the inputs having even numbers of ones.

A	B	$y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

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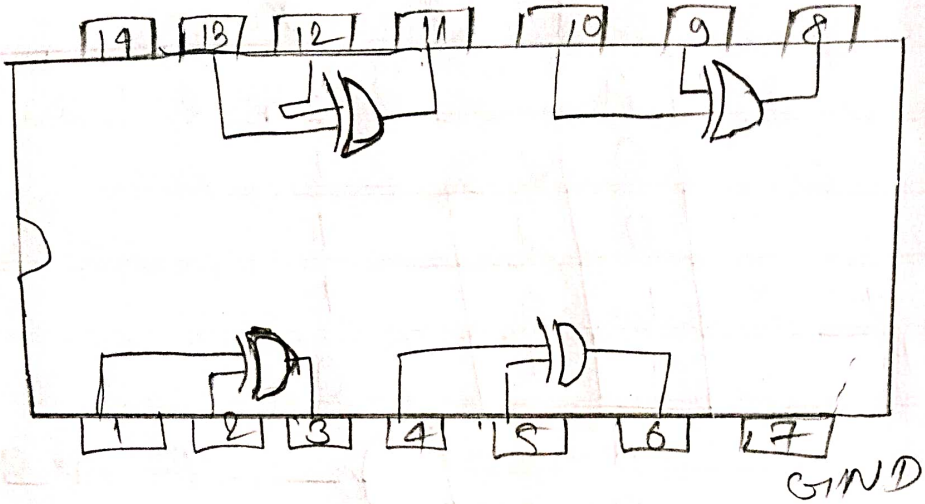
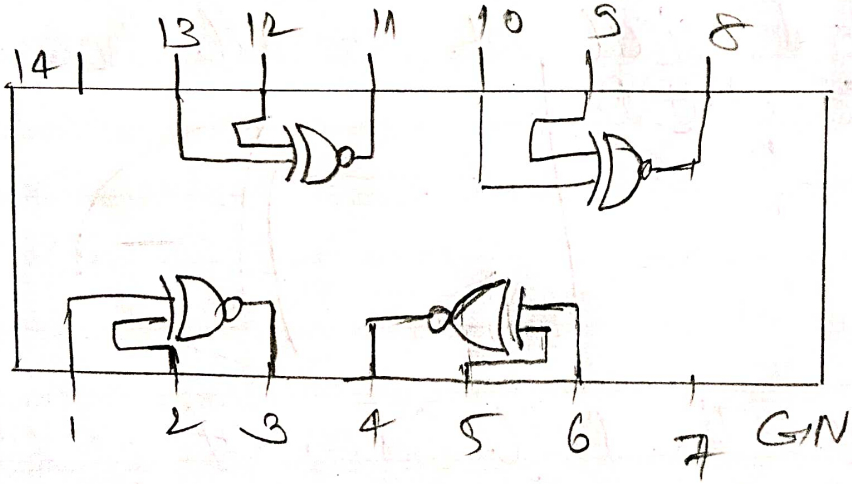
EX-OR gate



IC 7486

Ex-nor gate



IC 74266

XNOR - 74266

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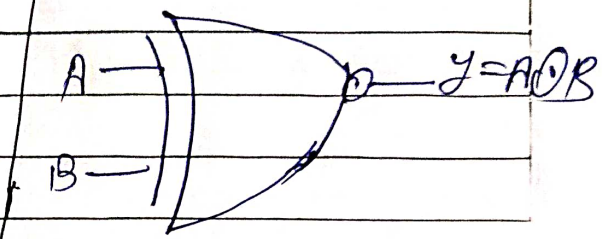
Ex-NOR gate: The full form of Ex-NOR gate is exclusive-NOR gate. Its function is same as that of OR gate except for some cases, when the inputs.

A	B	$Y = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1



Procedure: 1. Check the components for their working
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in circuit diagram.
4. Provide the input data via the input switches and observe output on output LED's.

Precautions:

1. Properly insert and remove the IC's in the breadboard.
2. Connections should be neat and clean.
3. Apply GND at pin number 7 and Vcc at pin number 14 of both IC's.

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Experiment 2: Realistion of Boolean function.

* Aim :- To simplify the given expression and to realize it using basic gate.

* objective:- 1) To simplify the Boolean expression and to build the logic circuit.

2. Given a truth table to derive the Boolean expressions and build the logic circuit to relize it.

* Components Required :- IC 7400, IC 7408, IC 7432 IC 7406, IC 7402 Connecting wire, Bread board.

* Theory: Canonical form : Any boolean function can be written in disjunction normal form (sum of min terms) or (product of max terms) A - boolean function can be represented by K- map. in which each cell corresponds to a minterm. The cells are arranged in such a way that any two adjacent cells corresponds to a minterm of distance.

Using Basic Gates / Nand Gate

NAND GATE AS NOT GATE,

Output is $Y = (A \cdot A)' = A'$

* NAND GATE AS AND GATE.

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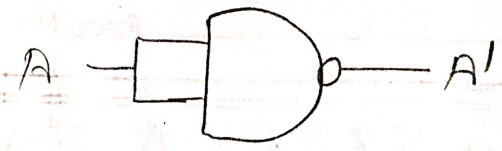
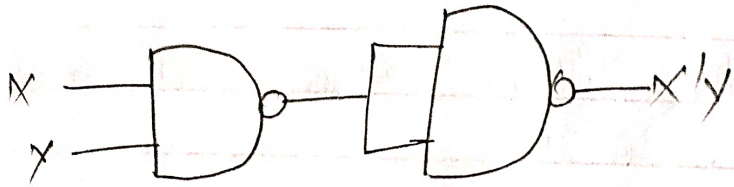
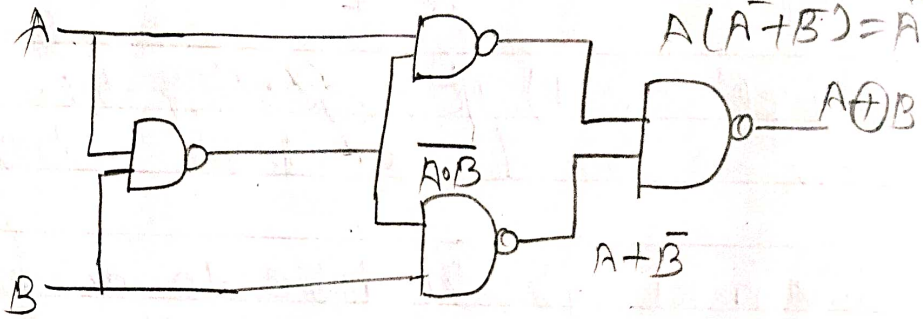
NAND GATE



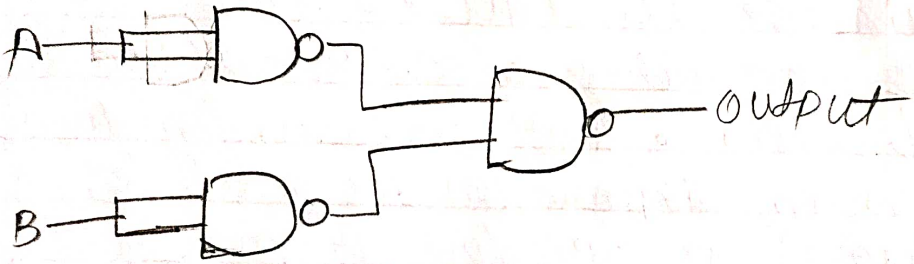
AS AND GATE



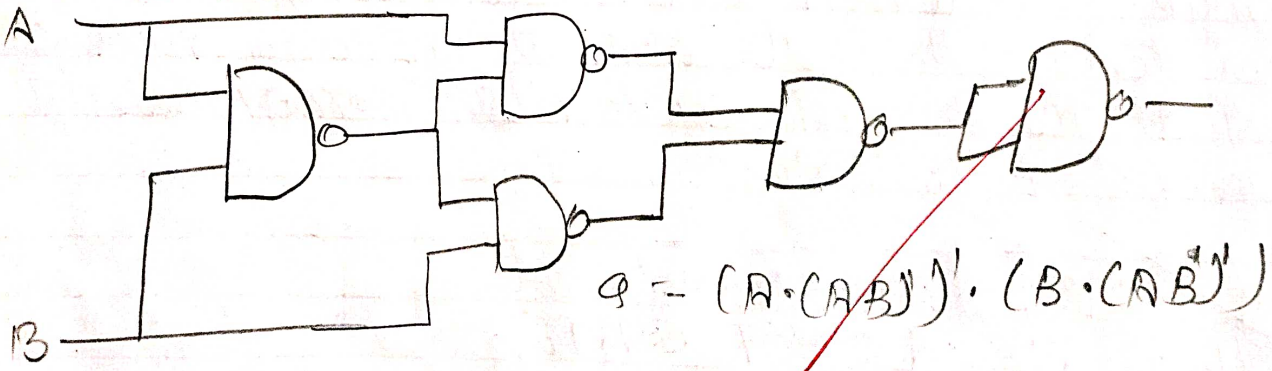
AS XOR GATE



AS OR GATE



AS X-NOR GATE



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$(A \cdot B)\, A' + B' = A + B$

- NAND GATE AS XOR GATE:

$$Y = (A(AB)')'\,(B(AB)')'$$
$$(A(AB)') + (B(AB)'))''$$
$$(A(A' + B')) + (B(A' + B'))$$
$$(AA' + AB') + (BA' + BB')$$
$$(0 + AB' + AB' + 0)$$
$$AB' + BA'$$
$$\boxed{Y = AB' + A'B}$$

- NAND AS X-NOR Gate: $y = AB + A'B'$
- NAND GATE AS NOR GATE: $y = (A + B)'$
  UNIVERSAL GATE / NOR
- NOR AS NOT: $y = (A + A)'$
  $Y = A'$
- NOR AS OR: $Y = (A + B')''$
- NOR AS AND: $(A + B)' = A'B'$
  $(A' + B') = A''B'' = AB$
- NOR AS XNOR: $Y = ((A + (A + B'))\,(B + (A + B)')')'$
  $(A + (A + B)')'' \cdot (B + (A + B)'))''$
  $(A + (A + B)') \cdot (B + A' \cdot B')$
  $(A + A'B') \cdot (B + A'B')$
  ~~$(A + A'B') \cdot (B + A'B')$~~ $(A + A') \cdot (A + B') \cdot (B + A')(B + B')$
  $AB + B'A'$
  $y = AB + A'B'$

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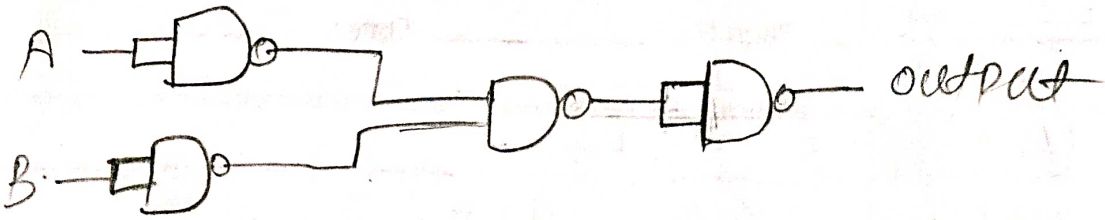
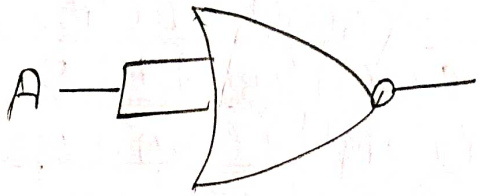
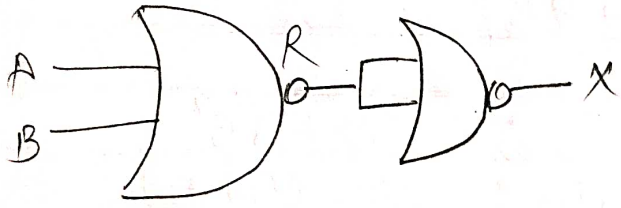


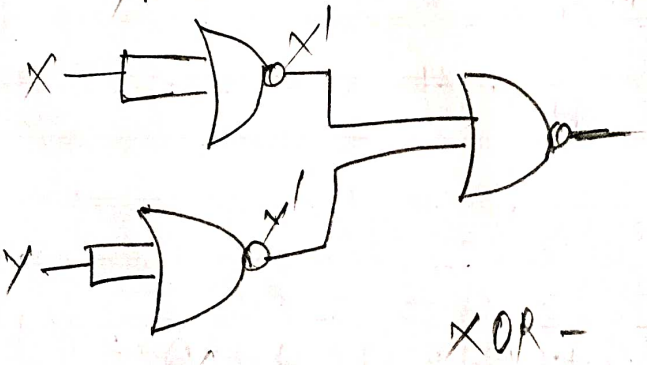
NOR GATE

① NOT → 

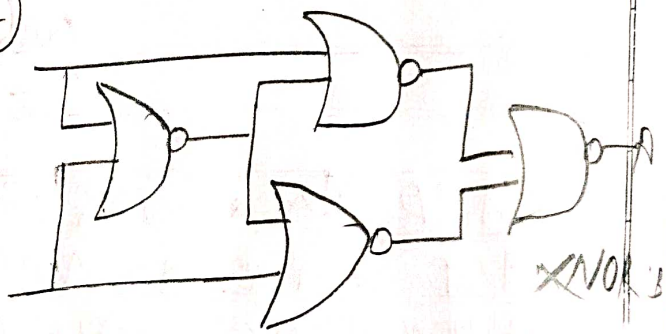
② OR



③ AND

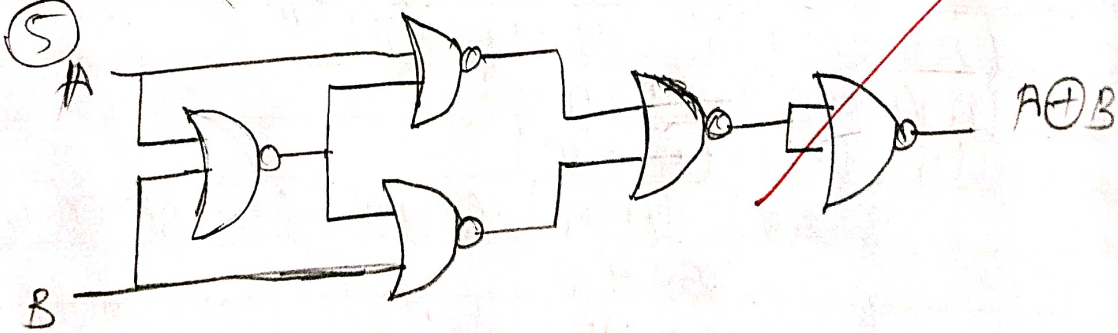


④ X-NOR



XOR - $y = A'B + AB'$

⑤



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- NOR AS X-OR : $Y = A'B + AB'$
- NOR AS NAND : $Y = (AB)'$

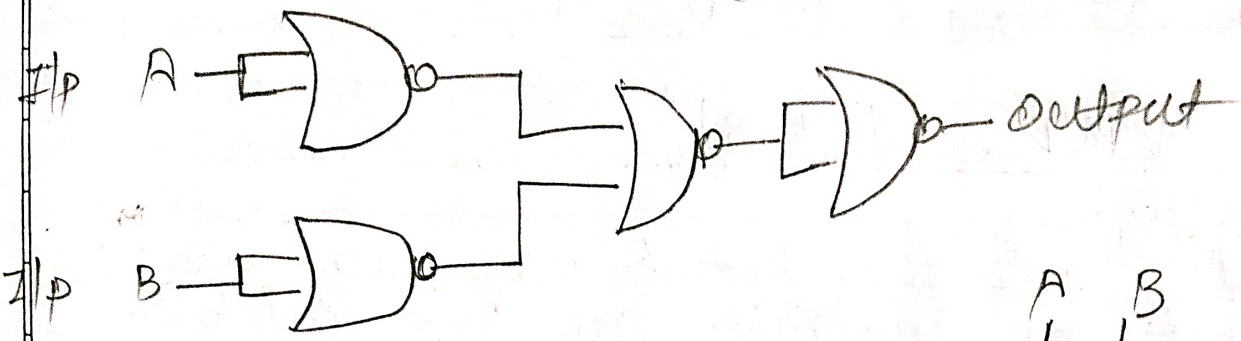
procedure :-

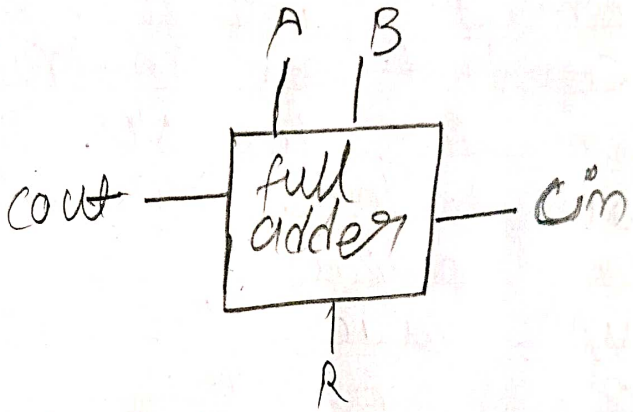
1. Connect the trainer kit to ac power supply.
2. ~~Construct an~~ Construct an R-S catch by converting two NOR gates as per logic diagram.
3. Connect logic sources to R, S input and Output Q, Q' outputs.
4. Apply various R-S combinations and observe Q, Q' output.
5. Verify the truth table.
6. Switch off ac power supply.

Teacher's Signature : _____

NOR GATE AS NAND GATE

$Y = (AB)'$





Truth table

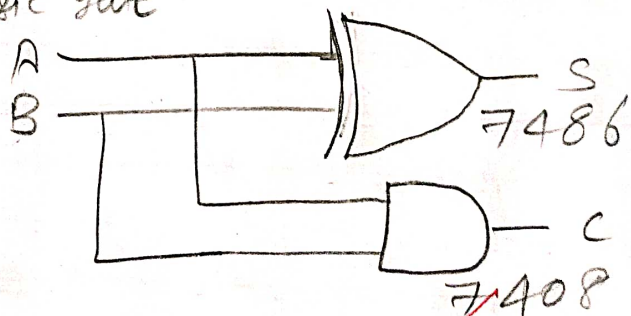
Input		output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean expression

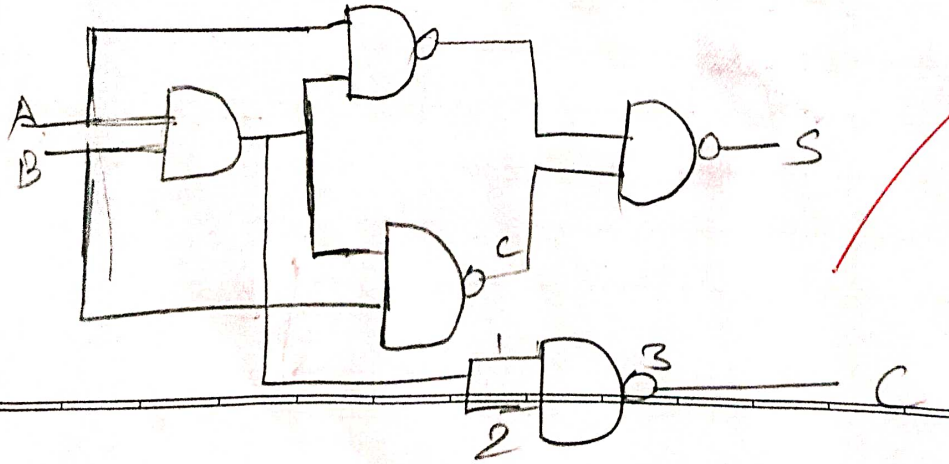
$S = A \oplus B$

$C = AB$

Basic gate



Nand gates.



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Experiment - 3

Half Adder | full Adder

Aim: To realise Half adder and full adder: Realisation using basic and XOR gates IC's.

Learning objective: - To realise the adder and circuits using basic gates and universal gates.

- To realize full adder using two half adders.
- Components required IC 7408, IC 7486, path cords and IC trainer kit

Theory: Half Adder → A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The help adder is able to add two single binary digit and provide output + carry. It has 2 inputs A, B and two output S(sum) and carry (C).

full adder: It is the adder which adder these inputs and procedure with two output. The first two input are A and B and third input is an C-IN C-out is normal output is designated as S which is SUM.

Teacher's Signature : _____

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A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another.

procedure :- check components for its working
- Insert appropriate IC's in IC base.
- Make Connections as shown in circuit diagram
- verify the truth table and observe the outputs

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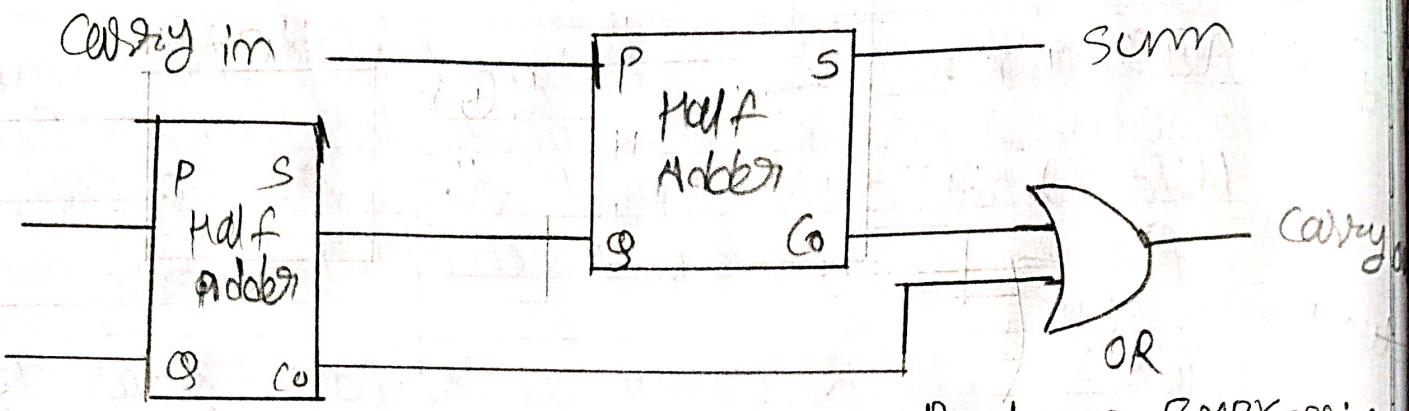
Full Adder from Half Adder



Truth Table of full adder

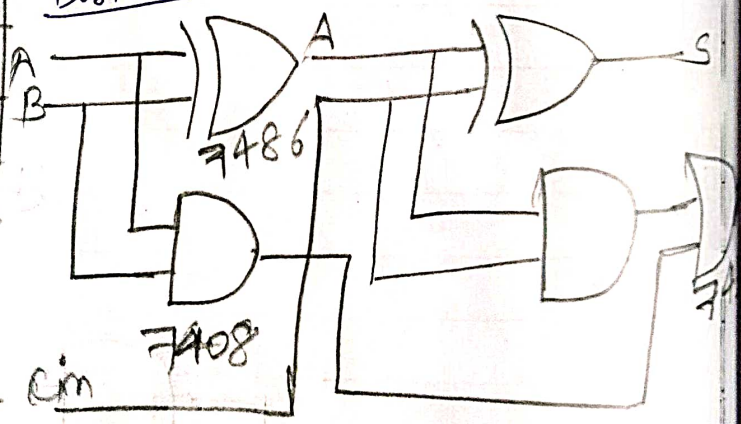
Input			output	
A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression

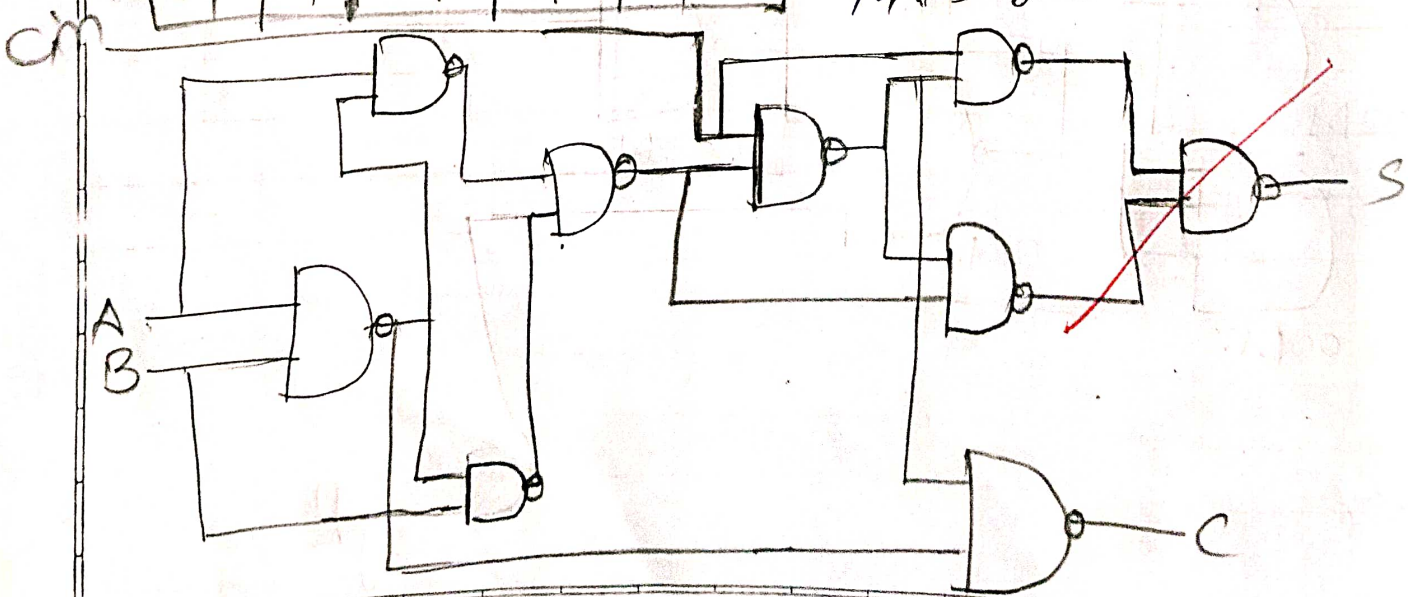
$S = A \oplus B \oplus C$

$C = AB + B\,C_{in} + A\,C_{in}$

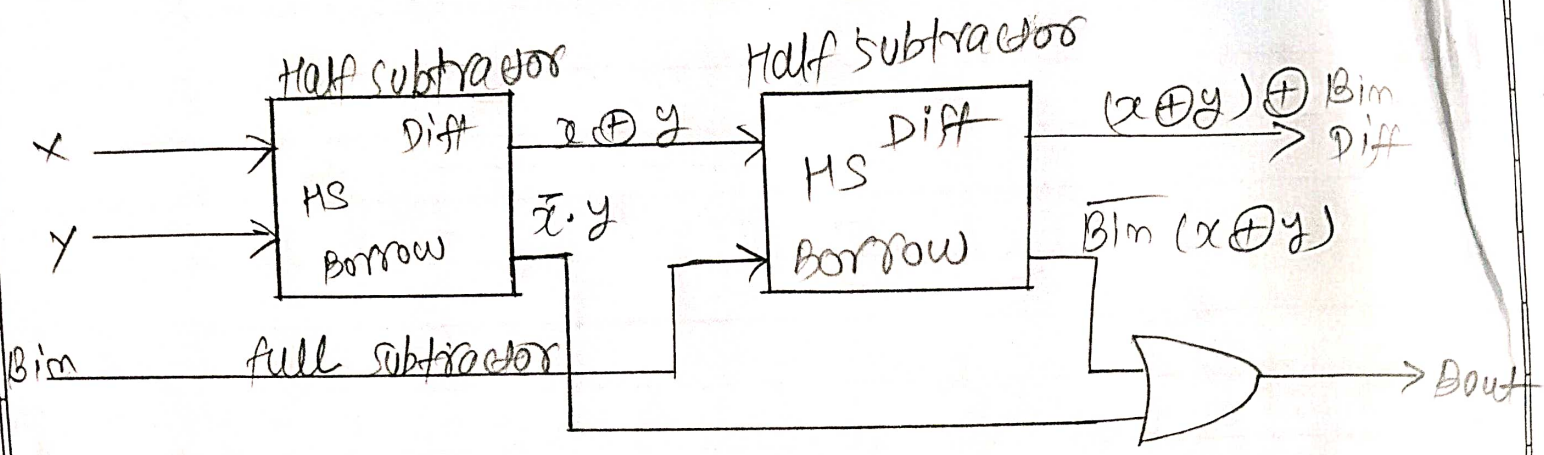
Basic gate

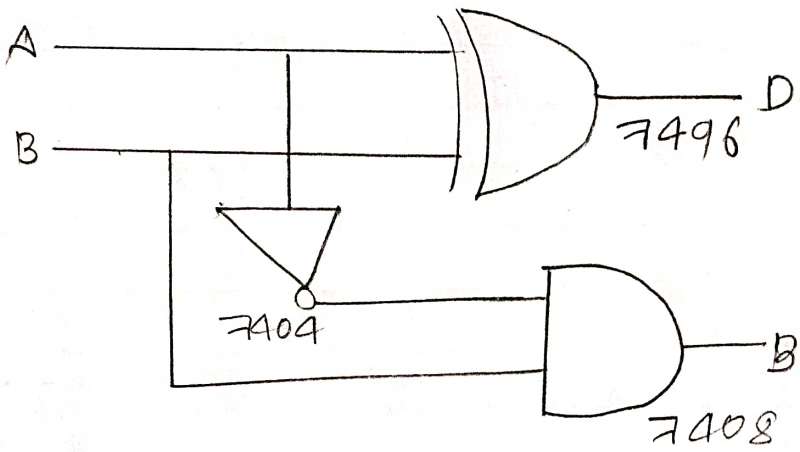


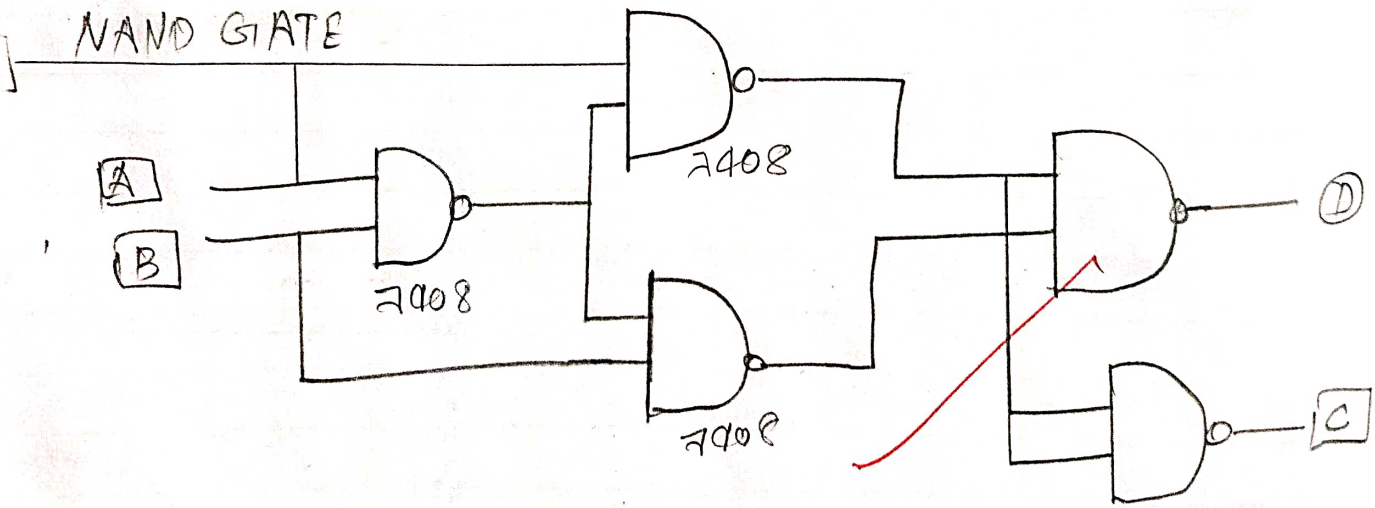
NAND gate



Full subtractor from Half subtractor







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Experiment : 4 :

Half subtractor / full subtractor

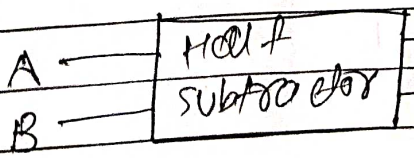
Aim : To realize half and full subtractor using IC's 7400 and 7402.

objective : To realize the subtractor circuits using basic gates and universal gates.

- To realize a full subtractor using two half subtractor.

Components Required : IC 7400, IC 7402, Patch Cord and Ic Trainer kit.

Theory : Half subtractor : It is a combinational circuit and as it name goes it is used to subtract two bits from the input. Here the output of the subtractor is purely deferent on present inputs and it doesn't depend on previous stages o/p's are borrow and differemce.



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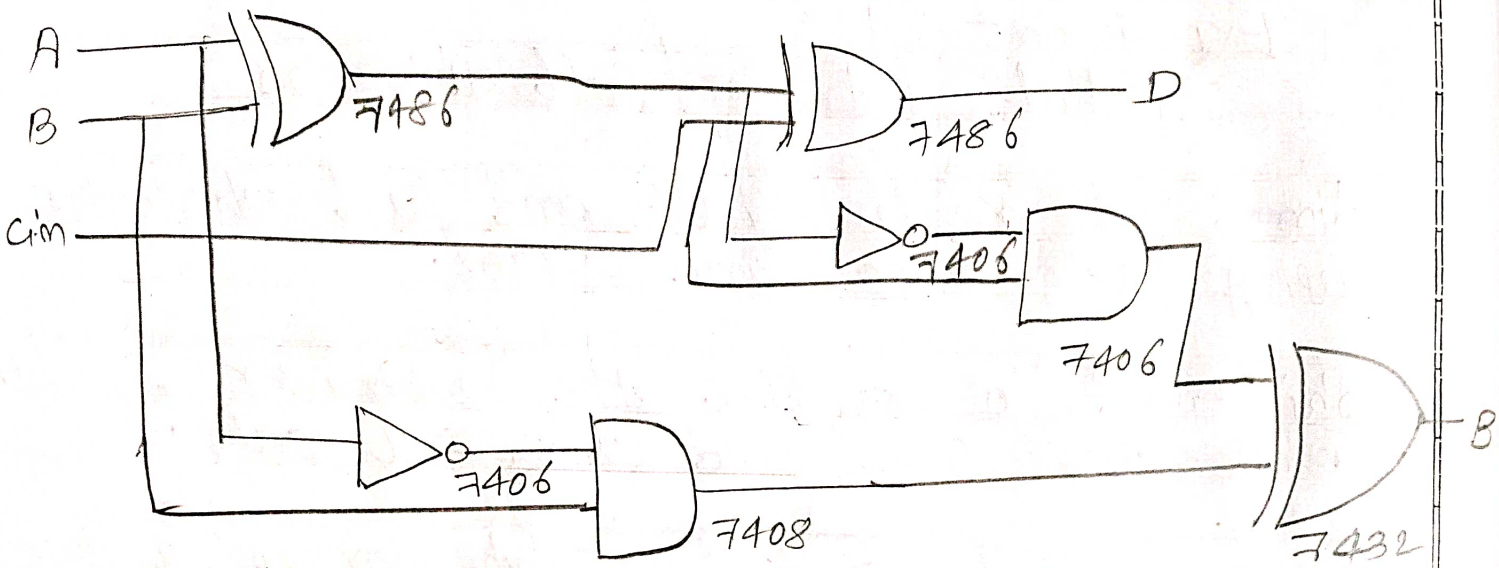
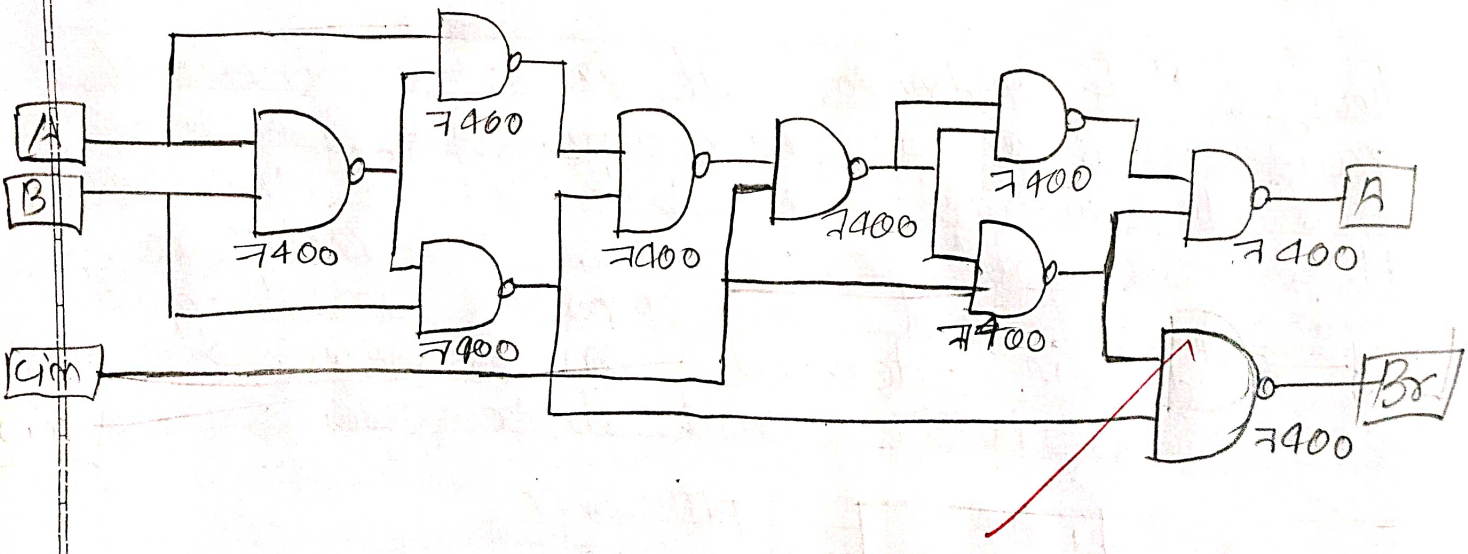
Full Subtractor

Basic gate



NAND GATE



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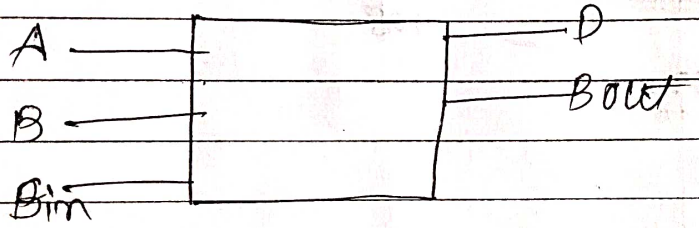
Full subtractor : It is combinational circuit that perform subtraction of two bits, one is minuend and other is ~~subter~~ subtrahend, taking into account borrow of the previous adjacent lower minuend bit. This circuit has 3 inputs and two outputs.



Half subtractor truth table

inputs		outputs	
A	B	D	Br
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Boolean expression

$D = A \oplus B$

$Br = A'B$

Full subtractor

Boolean Expression

$D = A \oplus B \oplus C$

$Br = A'B + BCin + A'Cin$

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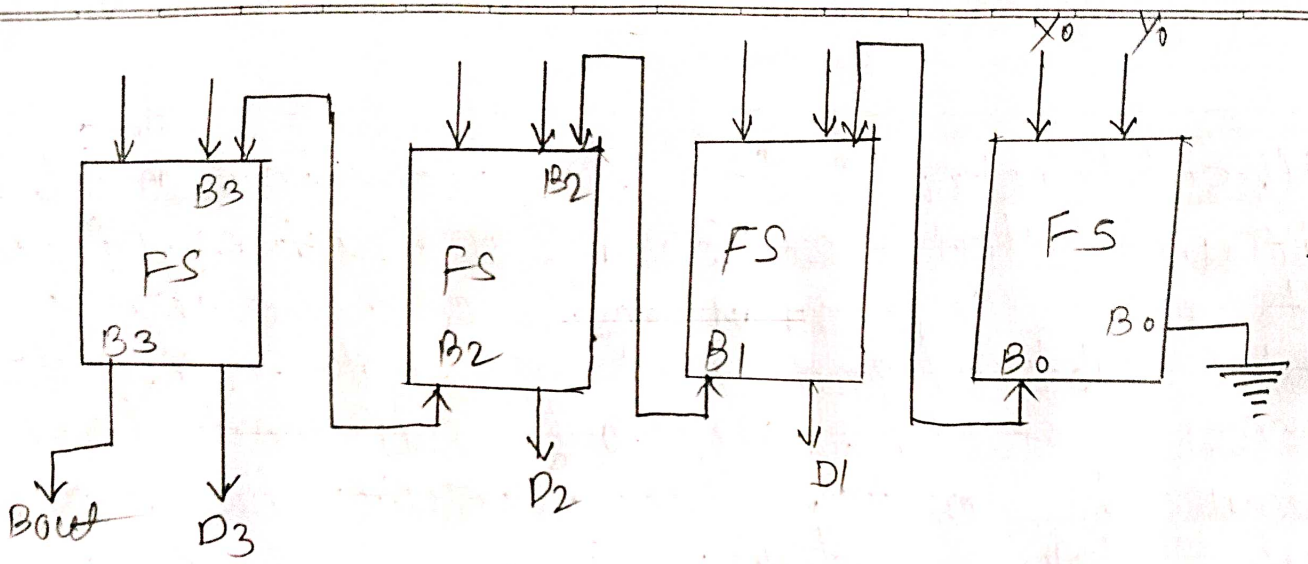
X_0
Y_0
B_3
FS
B_3
B_2
FS
B_2
FS
B_1
FS
B_0
B_0
B_{out}
D_3
D_2
D_1

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Truth table

Inputs		Output		
A	B	Cin	D	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Procedure: ① check component for its working.
② Insert appropriate IC's in IC base.
③ Make connection as shown in circuit diagram.
④ Verify truth table and observe o/p's.

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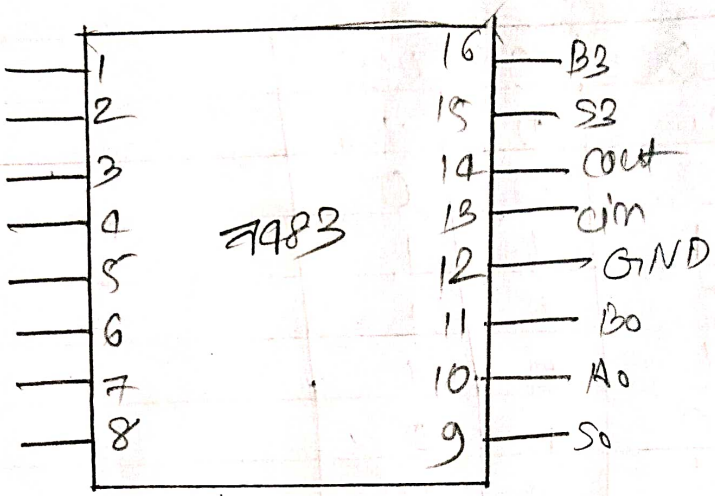
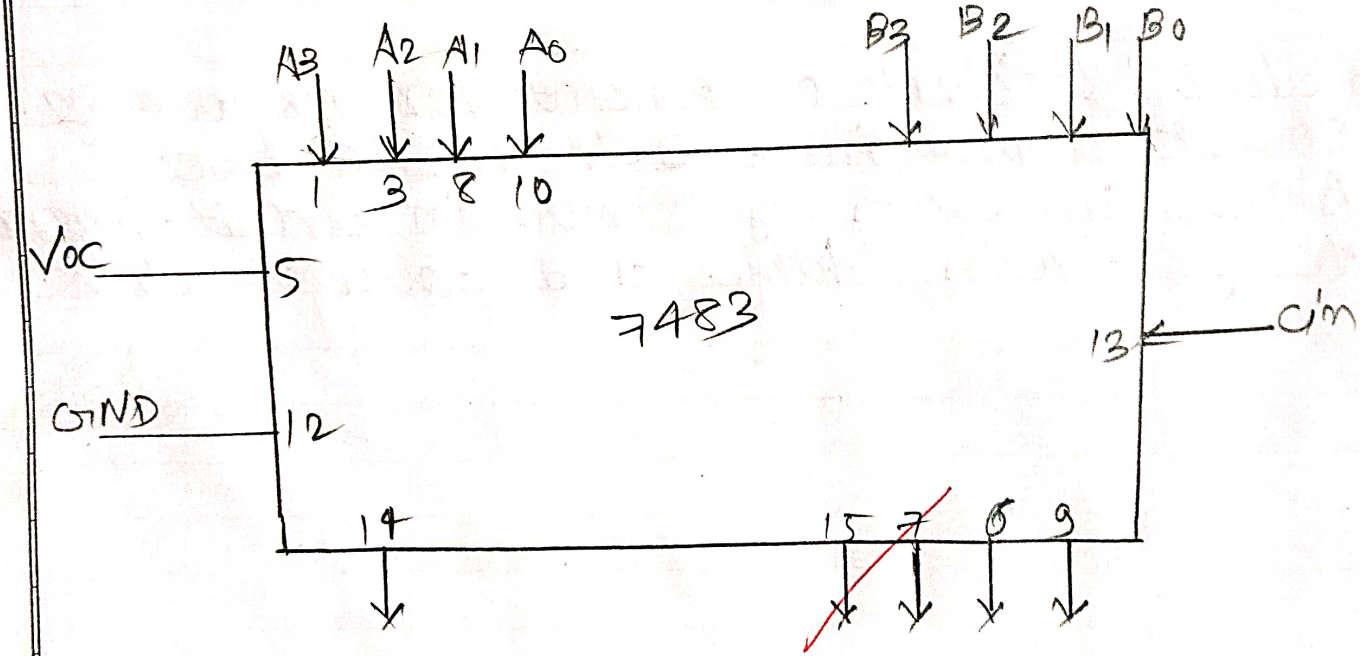

1
2
3
4
5
6
7
8
7483
16
15
14
13
12
11
10
9
B3
S3
Cout
Cin
GND
B0
A0
S0


A3
A2
A1
A0
B3
B2
B1
B0
1
3
8
10
Vcc
5
7483
13
Cin
GND
12
14
15
7
6
9

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Experiment - 5

~~Parallel~~ Parallel Adder / subtractor

Aim: Realisation of IC 7483 as parallel Adder subtractor.

Components Required: IC 7483 patch cords and IC Trainer kit.

Theory: 4 Bit Parallel Adder

The IC 7483 is a commonly available TTL 4-bit parallel binary adder chip. It Contains four interconnected full-adders and a look-ahead carry circuits for its operation. The & logic symbol of IC 7483 is show It has 4-bit Inputs $X_3X_2X_1X_0$ and $Y_3X_2X_1Y_0$, and a carry input cin in LSB stage, The O/P's are a 4-bit sum S_3 S_2 S_1 S_0 and a carry input Cin in LSB Stage. The O/P's are a 4-bit sum S_3, S_2, S_1, S_0 and a carry output Cout from the most significant bit stage.

Diagram show connection of two 7483 adders. The four least significant bits of the numbers are added in first adder carry

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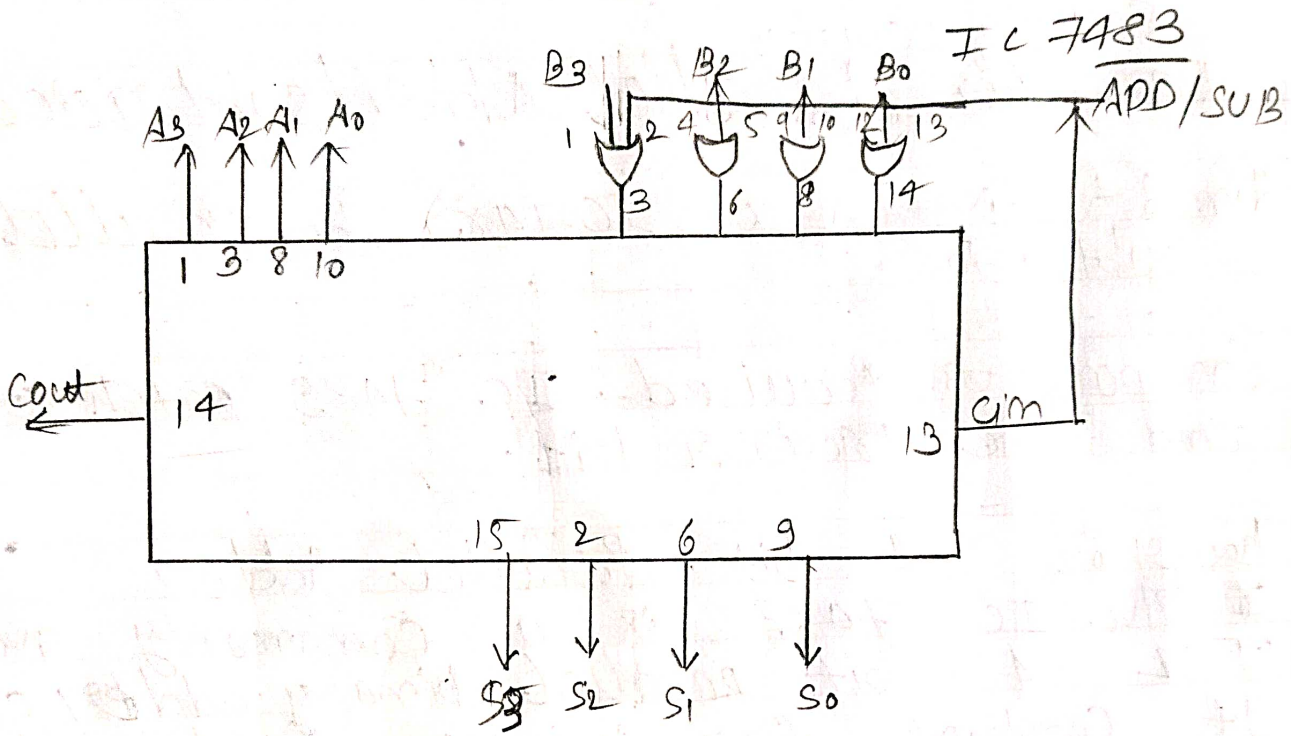
4-bit parallel binary adder/subtractor using



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O/p is given as carry I/P of second adder. The output of second adder is final carry output.

4 bit parallel subtractor

4-bit parallel Binary subtractor just a parallel binary adder can be implement by cascading several full-adders can also be implemented by cascading several full-subtractor A 4-bit parallel binary subtractor that subtracts a 4 bit number $Y_3Y_2Y_1Y_0$ from another 4-bit number $X_3X_2X_1X_0$. It has 4 difference O/P's $D_3D_2D_1D_0$ and borrow output (Bout). Note that the Bin of LSB full subtractor is connected too and Bout of 1st full-subtractor is connected to Bin of (i+1) th full subtractor.

Procedure:

1. check the components for its working
2. Insert appropriate IC's in IC Base.
3. Make connections as shown in circuit diagram.

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Experiment 6: Code converter

gray to Binary And Binary to gray converter

Aim: 4-Bit Binary to gray and gray to Binary code converter: Realization using Basic XOR, gates and Universal gates.

Components Required: Ic 7486 patch code and Ic Trainer kit.

Theory: Binary to gray code converter ~~binary to~~ The logical circuit which converts the binary code to equivalent gray code is known as binary to gray code converter. An n-bit gray code can be obtained by reflecting an n-1 bit code about an axis after 2^{n-1} rows and putting the MSB of 0 above the axis and MSB of below the axis. Reflection of gray codes are known.

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Decimal Number	4 bit Binary NO	4-bit gray code
	A B C D	G1 G2 G3 G4
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0

It means 4-bit gray code (4-1) or 3-bit code reflected against the axis drawn after (2^{4-1})th or 8th row

gray to Binary code converter → In gray to binary code converter, the input is gray code and output is equivalent binary code.

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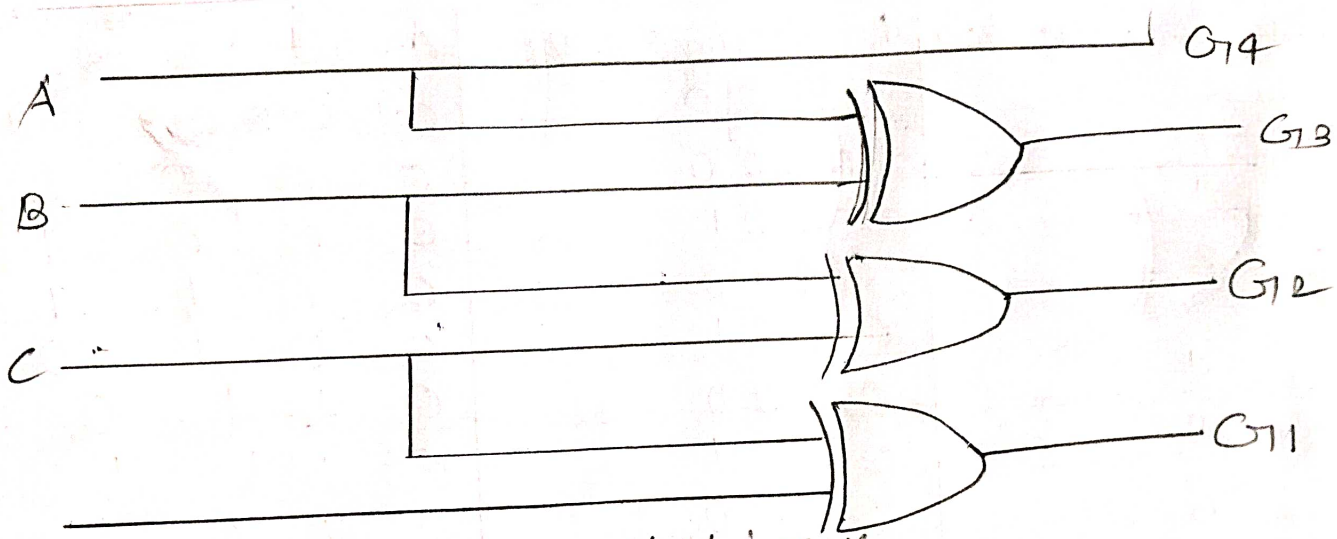
Binary to gray code converter



Gray to binary

4 bit gray code

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0

4 bit Binary code

B4	B3	B2	B1
0	0	0	0
0	0	0	1
0	0	0	1
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

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Let us consider a 4-bit gray to binary code converter. To design a 4 bit gray to binary code converter

procedure: Binary to gray ① The MSB of gray code will be exactly equal to first bit of given number.

② The second bit of code will be XOR of first and second bit of given binary no, if both the bit are same the result will be 0 and if they are different result will be 1.

③ The third bit of gray code will be equal to XOR of the second and third bit of given binary number. Thus binary to gray code conversion goes on.

④ Gray to binary: ① The MSB of the binary no will be equal to the MSB of the given gray code.

② Now if second gray bit is 0, then secondary bit will be same of it was. If it will 0. vice-versa.

③ This is gray to binary conversion.

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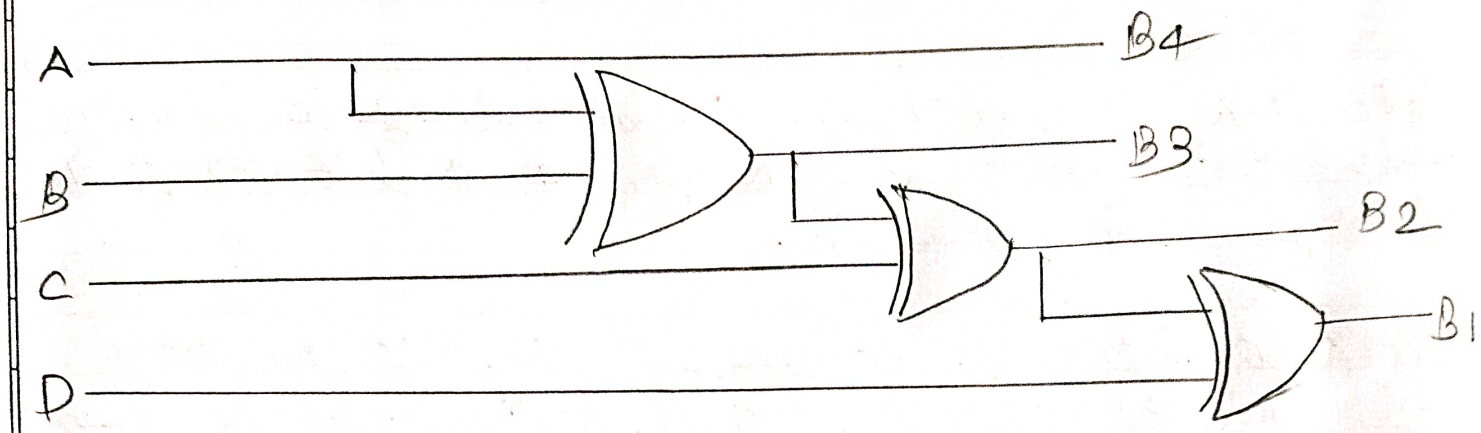

logic circuit for gray to binary code converter

Binary